Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1-24. (*Canceled*).

25. (*New*) A circular buffer control circuit, comprising

a first number of circular buffer start registers;

a first number of circular buffer end registers, each associated with a different one of the circular buffer start registers; and

circular buffer control logic including

means for comparing a pointer to an address in a selected one of the circular buffer end registers, and

means for restoring the address in the one of the circular buffer start registers associated with the selected circular buffer end register if the pointer matches the address in the selected circular buffer end register.

26. (*New*) A circular buffer control circuit, comprising

a first number of circular buffer start registers;

a first number of circular buffer end registers, each associated with a different one of the circular buffer start registers; and

control logic that compares a pointer to an address in a selected one of the circular buffer end registers and restores the address in the one of the circular buffer start

registers associated with the selected circular buffer end register if the pointer matches the address in the selected circular buffer end register.

27. (*New*): A digital signal processor capable of executing looping instruction commands, comprising:

a register set; and

means for executing a loop instruction command a fixed number of times on a number stored in the register set, including

first means for executing a current instruction stored in a first portion of a first register within the register set,

second means for decrementing a loop count value stored in a second register within the register set, and

third means for executing another portion of the current instruction stored in a second portion of the first register and a third register within the register set.

28. (*New*): The digital signal processor of claim 27, further including means for exiting the loop instruction command when the loop count value reaches zero.

29. (*New*): A digital signal processor capable of executing looping instruction commands, comprising:

a register set; and

control logic that executes a loop instruction command a fixed number of times on a number stored in the register set, wherein the control logic

executes a current instruction stored in a first portion of a first register within the register set,

decrements a loop count value stored in a second register within the register set, and

executes another portion of the current instruction stored in a second portion of the first register and a third register within the register set.

30. (*New*): The digital signal processor of claim 29, wherein the control logic exits the loop instruction command when the loop count value reaches zero.